A Low Jitter 5.3-GHz 0.18-μm CMOS PLL Based Frequency Synthesizer

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Abstract - **A 5.3-GHz CMOS phase locked loop (PLL) based frequency synthesizer is reported. The PLL operates as an integer-*N* frequency synthesizer using a ring-type voltage controlled oscillator (VCO). The PLL based synthesizer operates from 4.9 to 5.3-GHz and achieves a phase noise of -121.9 dBc/Hz at 10-MHz offset frequency from the carrier for maximum oscillation frequency of 5.3-GHz. The ring VCO works from 4.21 to 5.46-GHz with a maximum power consumption of 4.7-mW. A completely ripple-free VCO control voltage is obtained using a current mirror current source in a charge pump loop filter. The PLL is implemented with TSMC 0.18-μm technology for GSM applications. The output rms jitter is 0.3% of the oscillator period. The total power consumption of this synthesizer is only 10-mW from a 1.8 V power supply.**

I. INTRODUCTION

The rise of modern wireless telecommunication systems has resulted in a constant demand for compact, low-cost and high power portable devices. The huge demand has prompted researchers to design single-chip gigahertz-range PLL-based frequency synthesizers using CMOS technology [1-6]. Though the monolithic implementation of all other building blocks are showing constant success, the integration of high-speed RF CMOS PLL with low power consumption and phase noise, is still a challenge. In this paper, the exact analysis and design of a PLL based frequency synthesizer is extended using the ring VCO, current mirror in the charge pump and analog divide-by-two prescaler. The ripple-free VCO input control voltage helps to minimize jitter and transient locking overshoot. A realistic simulation of this PLL based synthesizer is presented using CADENCE design tools.

II. ANALYSIS

The PLL based integer-*N* frequency synthesizer block diagram is shown in Fig. 1. This sequential, duty cycle insensitive phase and frequency detector (PFD) detects the differences in phase and differences in frequencies between the reference clock (φ_{data_in}) and the generated internal VCO clock (φ_{dclock}). The PFD has a constant phase error transfer characteristic over the range of input phase error up to ± 1 cycle (360°). The loop locks within a short time (3.8 μs) and remains stable due to the use of a precise loop filter. The instability and ripple in the control voltage is removed by designing a precise current mirror in the charge pump. The pull-in range of this 5.3-GHz low power VCO is adequate to cover the frequency variation of the oscillator with temperature and power supply variations. A high frequency and low power analog divide-by-two prescaler and divide by 64 digital ripple counter are used in this architecture.

Using charge pump configuration, the output current of PFD can be written as [2],

$$I_{PDI} = \frac{I_{pump} - (-I_{pump})}{4\pi} \times \Delta\Phi = K_{PDI}\Delta\Phi \quad (1)$$

where, $K_{PDI} = \frac{2 \times I_{pump}}{\Delta\varphi}$

The transfer function of the charge pump loop filter is given by,

$$V_{inVCO} = K_F I_{PDI} \quad (2)$$

where,

$$K_F = \frac{1 + j\omega RC_1}{j\omega(C_1 + C_2)\left[1 + j\omega R\frac{C_1C_2}{C_1 + C_2}\right]} \quad (3)$$

$$with \quad C_2 \approx 0, \quad K_F \approx \frac{1 + sRC_1}{sC_1}$$

The VCO oscillation frequency increases with the control voltage. The gain of the VCO can be written as,

$$K_{VCO} = 2\pi\frac{f_{max} - f_{min}}{V_{max} - V_{min}} \quad (4)$$

Considering the block diagram in Fig. 1 the phase transfer function is given by,

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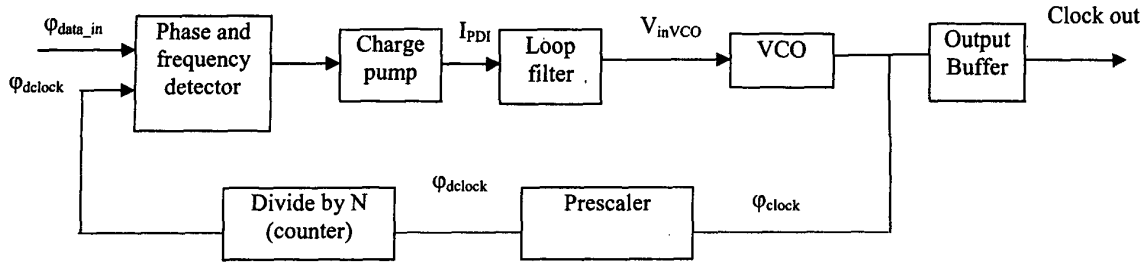

Fig. 1. Block diagram of PLL based frequency synthesizer

$$H(s)=\frac{\varphi_{clock}}{\varphi_{data}}=\frac{K_{PDI}K_F K_{VCO}}{s+\beta K_{PDI}K_F K_{VCO}} \quad (5)$$

$$H(s)=\frac{K_{PDI}K_{VCO}(1+sRC_1)}{s^2+\frac{s(K_{PDI}K_{VCO}R)}{N}+\frac{K_{PDI}K_{VCO}}{NC_1}} \quad (6)$$

From the transfer function the natural frequency (ω_n) and the damping factor (ζ) are given by

$$\omega_n=\sqrt{\frac{K_{PDI}K_{VCO}}{NC_1}} \quad ;\zeta=\frac{\omega_n}{2}RC_1 \quad (7)$$

The pull-in range is set by the VCO oscillator frequency range. The pull-in time is given by

$$T_P=2RC_1\ln\left[\frac{(K_{VCO}/N)(I_{pump})}{(K_{VCO}/N)(I_{pump})-\Delta\omega}\right] \quad (8)$$

The lock range of the closed loop system is

$$\Delta\omega=4\pi\zeta\omega_n=2\pi RC_1\omega_n^2 \quad (9)$$

The closed loop stability of this PLL-based frequency synthesizer is analyzed in the frequency domain (eq. 6). The mathematical formulation of the loop is verified numerically using the circuit parameters obtained from simulations using CADENCE simulation tool. The step response is shown in Fig. 2.

III. RESULTS AND DISCUSSION

This section describes the simulation results of the synthesizer using TSMC 0.18-μm CMOS technology. The VCO has a sensitivity of 1GHz/V which is shown in Fig. 3. The ring oscillator works in the range 4.21 to 5.46-GHz for a control voltage of 0.8 to 1.8V. The simulation includes the effect of parasitic capacitances and wire resistances. Fig. 4 shows the divide-by-2 prescaler and divide-by-64 ripple counter output that can divide upto 8.2- GHz. The total power consumed by the prescaler and the counter is only 5.1-mW. The locked external and internal clock waveforms are presented in Fig. 5.

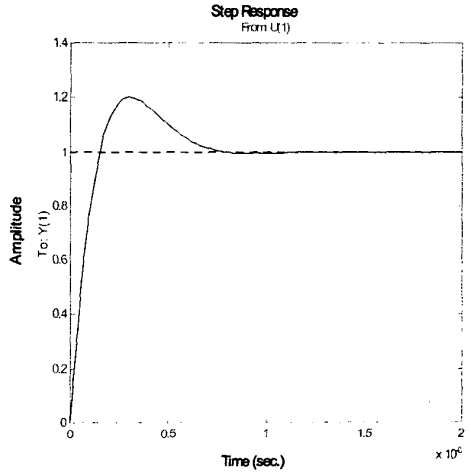

Fig. 2. Step response of PLL with N=128; f_{max} =5.3 GHz; f_{min} =4.9 GHz; V_{max} =1.8 V; V_{min} =0.9 V

This closed loop system reaches its locked state within a short pull-in time of 3.8 μs. Fig. 6 shows the maximum oscillation frequency 5.3 GHz. The input control voltage of the VCO as shown in Fig. 7, maintains a very steady dc value after locking.

The current mirror architecture current source used in the charge pump loop filter helps in averaging of the oscillator control voltage, which provides the zero over an entire update period. This feedforward zero helps this charge pump loop filter configuration to provide an absolutely ripple-free VCO input control voltage. The

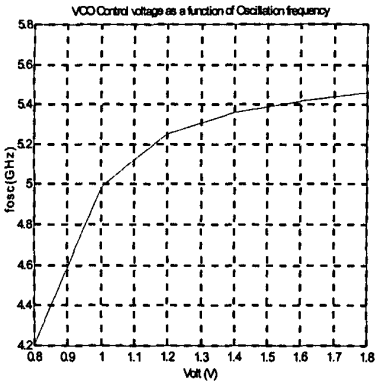

Fig. 3. VCO oscillation frequency as a function of control voltage

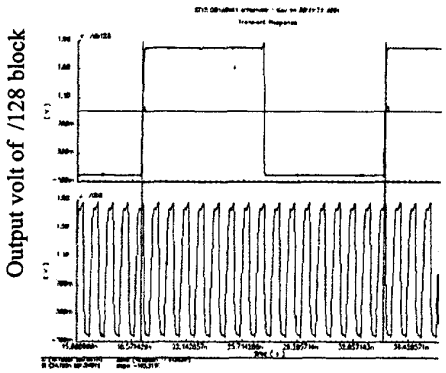

Fig. 4. Maximum operating frequency (8.2-GHz) of the prescaler

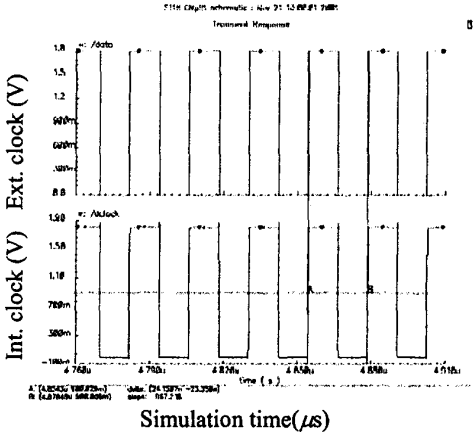

Fig. 5. External and generated internal clock

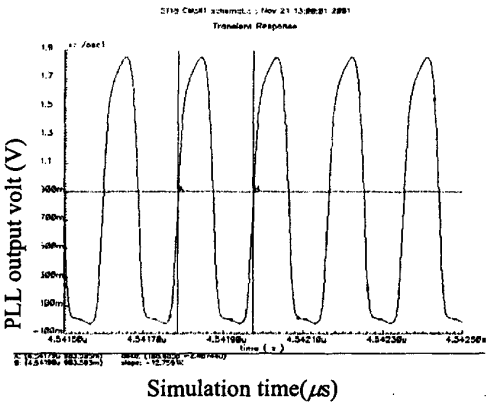

Fig. 6. Output oscillation frequency (5.3-GHz)

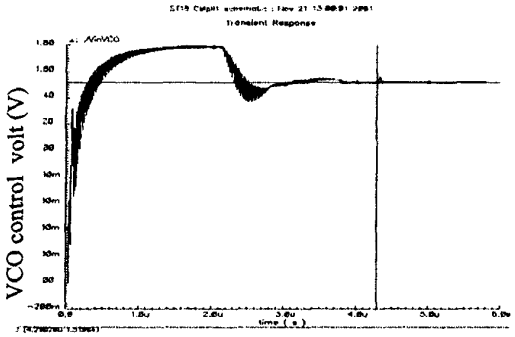

Fig. 7. Closed loop VCO input control voltage

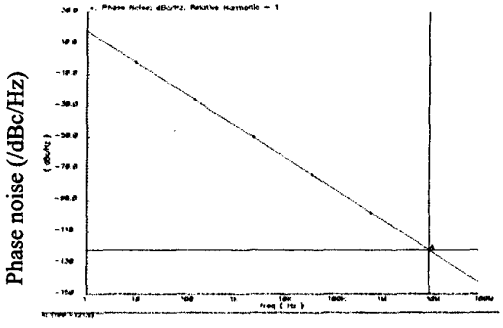

Fig. 8. Phase noise -121.9 dBc/Hz for oscillation frequency 5.3-GHz

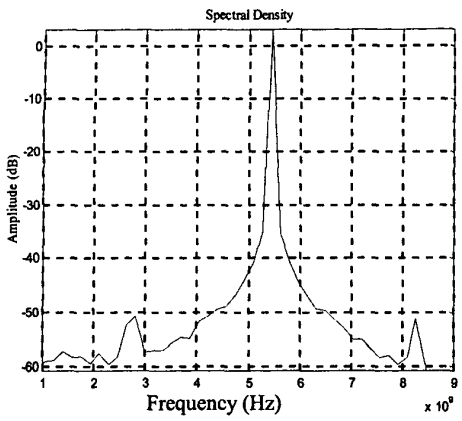

Fig. 9. Power spectral density at 5.3-GHz

need for an additional filtering pole is eliminated with the use of ripple-free control voltage, which leads to achieve a nearly 90^0 phase margin. As a result, input jitter and overshoot in transient locking are minimized. By choosing the proper damping factor of PLL, tracking is ensured between the stabilizing zero and the natural frequency. The bandwidth of PLL becomes high due to the use of lower time constants in the loop filter. The capacitance is smaller due to the lower time constants and the absence of the ripple filtering pole.

Fig. 8 shows the calculated phase noise of -121.9 dBc/Hz at 10-MHz offset frequency for an oscillation frequency of 5.3-GHz. Fig. 9 presents the power spectral density for the PLL operating at maximum frequency. The synthesizer consumes a total power of only 10-mW. The rms jitter is 0.3% of the oscillator period.

IV. CONCLUSIONS

A current mirror charge pump loop filter PLL design considering the effect of parasitic capacitance and wire resistances is reported in this paper. The current source is made insensitive to supply variations using current mirror in the charge pump. As a result, the modulation of VCO input control voltage is completely eliminated. The ripple-free control voltage provides low jitter and no overshoot in transient locking. The estimated component parameter values are all within the range of an on-chip implementation. The damping factor of the synthesizer is dependent only on the ratios of circuit components. A further optimization of the component values has been applied in order to ensure highest speed of 5.3-GHz and lowest power consumption of 10-mW, reported for the first time using this architecture. The mathematical derivation and closed loop simulation results have been verified using numerical analysis.

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